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| EXAMINER | |
|---|---|
| GAGLIOSTRO, KEVIN M | |
| **ART UNIT** | **PAPER NUMBER** |
| 2615 | |

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/046,402 | MABUCHI ET AL. | |
| | Examiner | Art Unit | |
| | Kevin M. Gagliostro | 2615 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on ~~15~~ 14 January 2001.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-25 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 15 January 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. 10/046,402.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

### *Claim Objections*

1. Claim 8 is objected to because of the following informalities: "portoin" and "egion" are misspelled. Appropriate correction is required.

### *Specification Objections*

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: "A MOS Type Solid-State Image Pickup Device and Driving Method Comprised of a Photodiode, a Detection Portions, and a Transfer Transistor."

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for rejections under this section made in this office action:

> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 4-5, 10, 14-15, 18-21, and 24-25 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,892,253 to Merrill.

   Merrill clearly shows all of the limitations cited in claim 1. See all material cited in the specification. Referring to claim 1, Merrill describes a solid-state image pickup device including pixels each of which comprises a photodiode (otherwise known as a semiconductor device that converts light to electrical current) (figure 2, item 50) and (column 2, lines 39-41). Merrill describes a detection portion, which is comprised of an n-type region (or n+ region, item 16), a transfer transistor (or, in the case, a source-follower transistor, item 26), and a read-out means of the collected total signal charge (figure 1) and (column 2, lines 17-23), which originated from the photodiode. Merrill also describes this transferring of charges wherein a gate voltage of said transfer transistor, when the charges are accumulated in said photodiode, is set to a negative voltage. Specifically, Merrill describes the negative voltage being applied to a photogate (PG) (figure 1, item 18) and (column 2, lines 7-9).

   Merrill clearly shows all of the limitations cited in claim 2. See all material cited in the specification. Referring to claim 2, Merrill describes the solid-state image pickup device as claimed in claim 1, wherein the negative voltage is set to a voltage under which a channel portion below the gate (or photogate (PG) 18) of said transfer transistor (or source-follower transistor 16) is inverted (column 2, lines 5-16).

Merrill clearly shows all of the limitations cited in claims 4 and 20. See all material cited in the specification. Referring to claims 4 and 20, Merrill describes a solid-state image pickup device (claim 4) and a method of driving a solid-state image pickup device (claim 20) including pixels each of which comprises a photodiode (otherwise known as a semiconductor device that converts light to electrical current) (figure 2, item 50) and (column 2, lines 39-41). Merrill describes a detection portion, which is comprised of an n-type region (or n+ region, item 16), a transfer transistor (or, in the case, a source-follower transistor, item 26), and a read-out means of the collected total signal charge (figure 1) and (column 2, lines 17-23), which originated from the photodiode. Merrill also describes this transferring of charges wherein a gate voltage of said transfer transistor, when the charges are accumulated in said photodiode, is set to a positive voltage. Specifically, Merrill describes the positive voltage being applied to a photogate (PG) (figure 1, item 18) and (column 1, lines 54-57).

Merrill clearly shows all of the limitations cited in claims 5 and 21. See all material cited in the specification. Referring to claims 5 and 21, Merrill describes a solid-state image pickup device as claimed in claim 4 and a solid-state image pickup device driving method as claimed in claim 20, wherein the positive voltage is set to a voltage under which a channel portion below the gate (transfer gate 20) (column 2, lines 5-9).

Merrill clearly shows all of the limitations cited in claim 10. See all material cited in the specification. Referring to claim 10, Merrill describes the solid-state image pickup device including pixels each of which comprises a photodiode (otherwise known as a semiconductor device that converts light to electrical current) (figure 2, item 50) and (column 2, lines 39-41). Merrill describes a detection portion, which is comprised of an n-type region (or n+ region, figure 1, item 16), a transfer transistor (or, in the case, a source-follower transistor, item 26), and a read-out means of the collected total signal charge (figure 1) and (column 2, lines 17-23), which originated from the photodiode. Merrill further describes an overflow path for discharging charges overflowing from said photodiode is formed in a bulk out of a channel portion of said transfer transistor. Specifically, this is stated in Merrill as with a negative voltage applied to photogate (PG) (figure 1, item 18) in combination with a positive voltage on n+ region 16 causing the charges collected under the photogate (figure 1, item 18) (makes up part of photodiode region) to flow (overflow) through the inverted surface region under transfer gate (figure 1, item 20) (makes up channel portion) via n+ region (figure 1, item 14) to n+ region 16 (makes up the bulk out of the channel portion of transfer transistor) where each incoming electron reduces the initial transfer voltage on n+ region 16 to a final transfer voltage (column 2, lines 10-16).

Merrill clearly shows all of the limitations cited in claim 14. See all material cited in the specification. Referring to claim 14, Merrill describes method of driving a solid-

state image pickup device including pixels each of which comprises a photodiode (otherwise known as a semiconductor device that converts light to electrical current) (figure 2, item 50) and (column 2, lines 39-41). Merrill describes a detection portion, which is comprised of an n-type region (or n+ region, item 16), a transfer transistor (or, in the case, a source-follower transistor, item 26), and a read-out means of the collected total signal charge (figure 1) and (column 2, lines 17-23), which originated from the photodiode. Merrill also describes this transferring of charges wherein a gate voltage of said transfer transistor, when the charges are accumulated in said photodiode, is set to a negative voltage. Specifically, Merrill describes the negative voltage being applied to a photogate (PG) (figure 1, item 18) and (column 2, lines 7-9).

Merrill clearly shows all of the limitations cited in claim 15. See all material cited in the specification. Referring to claim 15, Merrill describes the solid-state image pickup device driving method as claimed in claim 14, wherein the negative voltage is set to a voltage under which a channel portion below the gate (or photogate (PG) 18) of said transfer transistor (or source-follower transistor 16) is inverted (column 2, lines 5-16).

Merrill clearly shows all of the limitations cited in claims 18 and 24. See all material cited in the specification. Referring to claims 18 and 24, Merrill describes the solid-state image pickup device driving method as claimed in claim 14 (claim 18) and the solid-state image pickup device driving method as claimed in claim 20 (claim 24), wherein charge overflowing from said photodiode are discharged to the detection portion side through the lower side of the channel portion of said transfer transistor. Specifically, this is stated in Merrill as with a negative voltage applied to photogate (PG) (figure 1, item 18) in combination with a positive voltage on n+ region 16 causing the charges collected under the photogate (figure 1, item 18) (makes up part of photodiode region) to flow (overflow) through the inverted surface region under transfer gate (figure 1, item 20) (makes up channel portion) via n+ region (figure 1, item 14) to n+ region 16 (makes up the bulk out of the channel portion of transfer transistor) where each incoming electron reduces the initial transfer voltage on n+ region 16 to a final transfer voltage (column 2, lines 10-16). Also, Merrill describes a detection portion, which is comprised of an n-type region (or n+ region, item 16), a transfer transistor (or, in the case, a source-follower transistor, item 26), and a read-out means of the collected total signal charge (figure 1) and (column 2, lines 17-23), which originated from the photodiode.

Regarding claims 19 and 25 Merrill describes the solid-state image pickup device driving method as claimed in claims 14 and 20, further describing wherein charges overflowing from said photodiode are discharged to the detection portion side through the lower side of the channel portion of said transfer transistor. Specifically, this is stated in Merrill as with a negative voltage applied to photogate (PG) (figure 1, item 18) in combination with a positive voltage on n+ region 16 causing the charges

collected under the photogate (figure 1, item 18) (makes up part of photodiode region) to flow (overflow) through the inverted surface region under transfer gate (figure 1, item 20) (makes up channel portion) via n+ region (figure 1, item 14) to n+ region 16 (makes up the bulk out of the channel portion of transfer transistor) where each incoming electron reduces the initial transfer voltage on n+ region 16 to a final transfer voltage (column 2, lines 10-16). Also, Merrill describes a detection portion, which is comprised of an n-type region (or n+ region, item 16), a transfer transistor (or, in the case, a source-follower transistor, item 26), and a read-out means of the collected total signal charge (figure 1) and (column 2, lines 17-23), which originated from the photodiode. Merrill further describes charges overflowing from said photodiode and discharging through the lower side of the channel transfer portion of said transfer transistor (all described above) to the substrate side. Specifically, the n+ region 16 of Merrill (where the charges flow) is formed within the p-type substrate (figure 1, item 12), thus comprising the region where charges overflow to a substrate side (column 1, lines 32-42).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 103 that form the basis for rejections under this section made in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 3 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,892,253 to Merrill in view of U.S. Patent No. 5,650,340 to Burr et al.

Regarding claims 3 and 16 Merrill describes the solid-state image pickup device as claimed in claim 1 (claim 3) and the solid-state image pickup device driving method as claimed in claim 14 (claim 16), but does not teach the device wherein the negative voltage is set (-) 0.5 volts or less. Burr describes a voltage threshold ($V_T$) between (-) 150 and (+) 150 millivolts within a gate voltage ($V_{GS}$) for the embodiment of the invention (column 9, lines 21-25). Burr further describes that, due to processing variations, the exact dopant concentration (impurity concentration) in the channel region (under the gate) can vary from device to device. Within these variations, a change in threshold voltage ($V_T$) may vary by tens or even hundreds of millivolts (column 9, lines 49-55). With that said, the gate voltage ($V_{GS}$) must be capable of having a negative voltage of (-) 0.5 volts or less. Therefore, it would have been obvious to one of ordinary skill in the art to modify the solid-state image pickup device of Merrill to include a negative gate voltage, which is set to (-) 0.5 volts or less. One would have been motivated to combine the glare reduction device of Merrill to include the negative gate voltage of (-) 0.5 volts or less of Burr in that a

slight variation from device to device (causing significant change in the threshold voltages) is realistic in that there are variations in processing (column 9, lines 49-55).

7. Claims 7-9, 11-13, 17, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,892,253 to Merrill in view of U.S. Patent No. 5,714,782 to Nakagawa et al.

Regarding claims 7 and 11 Merrill describes the solid-state image pickup device as claimed in claims 1 and 10, but does not teach the device wherein an overflow path is formed of an area extended from the portion just below said photodiode to a semiconductor substrate and said area is formed of an n-type semiconductor region having an impurity concentration lower than that of a semiconductor well region or a p-type semiconductor region. Nakagawa describes semiconductor substrate formed of an n-type semiconductor region (or n-type active layer) (Nakagawa: figure 28, item 303) having an impurity concentration lower than that of a semiconductor well region (or a p-type base layer) (Nakagawa: figure 28, item 305) (Nakagawa: column 14, lines 15-25) and (Nakagawa: column 17, claim 1). Nakagawa further describes this n-type semiconductor region (n-type active layer 303) as a place where charges (current) are permitted to flow (overflow) (Nakagawa: column 14, lines 26-30). Particularly, Nakagawa does not describe this n-type active layer 303 as being formed in the area extended from the portion just below said photodiode to a semiconductor substrate. However, Nakagawa describes the n-type semiconductor region (or n-type buried layer 54) which is formed of a portion below the photodiode (PD) (Nakagawa: figure 13A, item PD and column 8, lines 56-65) reaching to semiconductor substrate (or p-type semiconductor substrate 51) (Nakagawa: figure 13A, item 51) which also follows the embodiment of charge flow, which is similar to that of n-type layer 303. Therefore, it would have been obvious to one of ordinary skill in the art to modify the solid-state image pickup device of Merrill to include the n-type semiconductor region impurity concentration being lower than the p-type semiconductor region and said region extending from just below the photodiode to the p-type semiconductor substrate. One would have been motivated to combine the solid-state image pickup device of Merrill to include the n-type region impurity concentration lower than the p-type region and n-type region extending from below the photodiode to the p-type substrate of Nakagawa in that this embodiment would make it possible to realize a low on-state voltage even when a large current is caused to flow (Nakagawa: column 14, lines 26-31).

Regarding claims 8 and 12 Merrill describes the solid-state image pickup device as claimed in any one of claims 1 and 4, and in claim 10, but does not teach the device wherein said overflow path is formed in the area between said photodiode and said detection portion in each pixel is formed of an n-type semiconductor region having an impurity concentration lower than that of a semiconductor well region or a p-type semiconductor region. Nakagawa describes semiconductor substrate formed of an n-type semiconductor region (or n-type active layer) (Nakagawa: figure 28, item 303)

having an impurity concentration lower than that of a semiconductor well region (or a p-type base layer) (Nakagawa: figure 28, item 305) (Nakagawa: column 14, lines 15-25) and (Nakagawa: column 17, claim 1). Nakagawa further describes the n-type semiconductor region (or n-type buried layer 54), which is formed of a portion below the photodiode (PD) (Nakagawa: figure 13A, item PD and column 8, lines 56-65) reaching to semiconductor substrate (or p-type semiconductor substrate 51) (Nakagawa: figure 13A, item 51). Note that a photocoupler is integrally formed with the p-type semiconductor substrate 51 and functions as a current detection means of the current path, therefore comprising that of a detection portion. Since, the p-type semiconductor substrate 51 comprises that of a detection portion, then the n-type buried layer 54 does in fact fall between the area between said photodiode and the detection portion. Therefore, it would have been obvious to one of ordinary skill in the art to modify the solid-state image pickup device of Merrill to include the n-type semiconductor region impurity concentration being lower than the p-type semiconductor region and said overflow path is formed in the area between said photodiode and said detection portion. One would have been motivated to combine the solid-state image pickup device of Merrill to include the n-type region impurity concentration lower than the p-type region and n-type region being in the area between the photodiode to the p-type substrate of Nakagawa in that this embodiment would make it possible to realize a low on-state voltage even when a large current is caused to flow (Nakagawa: column 14, lines 26-31).

Regarding claims 9 and 13 Merrill describes the solid-state image pickup device as claimed in any one of claims 1 and 4 and as claimed in claim 10, but does not teach the device wherein an overflow path is formed of an area extending from the portion just below said photodiode and the area between said photodiode and said detection portion to a semiconductor substrate in each pixel is formed of an n-type semiconductor region having an impurity concentration lower than that of a semiconductor well region or a p-type semiconductor region. Nakagawa describes semiconductor substrate formed of an n-type semiconductor region (or n-type active layer) (Nakagawa: figure 28, item 303) having an impurity concentration lower than that of a semiconductor well region (or a p-type base layer) (Nakagawa: figure 28, item 305) (Nakagawa: column 14, lines 15-25) and (Nakagawa: column 17, claim 1). Nakagawa further describes this n-type semiconductor region (n-type active layer 303) as a place where charges (current) are permitted to flow (overflow) (Nakagawa: column 14, lines 26-30). Particularly, Nakagawa does not describe this n-type active layer 303 as being formed in the area extended from the portion just below said photodiode to a semiconductor substrate. However, Nakagawa describes the n-type semiconductor region (or n-type buried layer 54) which is formed of a portion below the photodiode (PD) (Nakagawa: figure 13A, item PD and column 8, lines 56-65) reaching to semiconductor substrate (or p-type semiconductor substrate 51) (Nakagawa: figure 13A, item 51) which also follows the embodiment of charge flow, which is similar to that of n-type layer 303. Keep in mind that this area described as "below the photodiode" simultaneously comprises that of the "area between said

photodiode and said detection portion," since the p-type semiconductor substrate 51 comprises that of a detection portion, then the n-type buried layer 54 does in fact fall between the area between said photodiode and the detection portion. Therefore, it would have been obvious to one of ordinary skill in the art to modify the solid-state image pickup device of Merrill to include the n-type semiconductor region impurity concentration being lower than the p-type semiconductor region and overflow path is formed of an area extending from the portion just below said photodiode and the area between said photodiode and said detection portion to a semiconductor substrate. One would have been motivated to combine the solid-state image pickup device of Merrill to include the n-type region impurity concentration lower than the p-type region and n-type region extending from below the photodiode to the p-type substrate of Nakagawa in that this embodiment would make it possible to realize a low on-state voltage even when a large current is caused to flow (Nakagawa: column 14, lines 26-31).

Regarding claims 17 and 23 Merrill describes the solid-state image pickup device driving method as claimed in claims 14 and 20, but does not teach the device wherein said charges overflowing from said photodiode are discharged to the substrate side. Nakagawa describes an n-type semiconductor region (n-type active layer 303) as a place where charges (current) are permitted to flow (overflow) (Nakagawa: column 14, lines 26-30). Particularly, Nakagawa does not describe this n-type active layer 303 as being formed in the area extended from the portion just below said photodiode to a semiconductor substrate. However, Nakagawa describes the n-type semiconductor region (or n-type buried layer 54) which is formed of a portion below the photodiode (PD) (Nakagawa: figure 13A, item PD and column 8, lines 56-65) reaching to semiconductor substrate (or p-type semiconductor substrate 51) (Nakagawa: figure 13A, item 51) which also follows the embodiment of charge flow, which is similar to that of n-type layer 303. Therefore, it would have been obvious to one of ordinary skill in the art to modify the solid-state image pickup device of Merrill to include charges overflowing from said photodiode that are discharged to the substrate side. One would have been motivated to combine the solid-state image pickup device of Merrill to include the n-type region impurity concentration lower than the p-type region and n-type region extending from below the photodiode to the p-type substrate of Nakagawa in that this embodiment would make it possible to realize a low on-state voltage even when a large current is caused to flow (Nakagawa: column 14, lines 26-31).

8. Claims 6 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,892,253 to Merrill in view of U.S. Patent No. 4,733,286 to Matsumoto.

Regarding claims 6 and 22 Merrill describes the solid-state image pickup device as claimed in claim 4 and the solid-state image pickup device driving method as claimed in claim 20, but does not teach the device wherein a positive voltage is set

to a power source voltage or more. Matsumoto describes a forward voltage bias applied to a gate electrode (figure 1, item 6) and (column 2, lines 2-6). Therefore, it would have been obvious to one of ordinary skill in the art to modify the solid-state image pickup device of Merrill to include a positive voltage on the gate that is set to a power source voltage or more. One would have been motivated to combine the positive voltage applied to the photogate (PG) (Merrill: figure 1, item 18) to include the forward voltage bias (or source voltage) being applied to the gate electrode of Matsumoto in that an output which is amplified with respect to the light output (photodiode) can now be obtained (Matsumoto: column 2, lines 6-8).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Gagliostro whose telephone number is 703-308-6070. The examiner can normally be reached on 8:00 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Christensen can be reached on 703-308-9644. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin Gagliostro 1/5/2005

NGOC-YEN VU
PRIMARY EXAMINER